Ternary Volatile Random Access Memory based on Heterogeneous Graphene-CMOS Fabric

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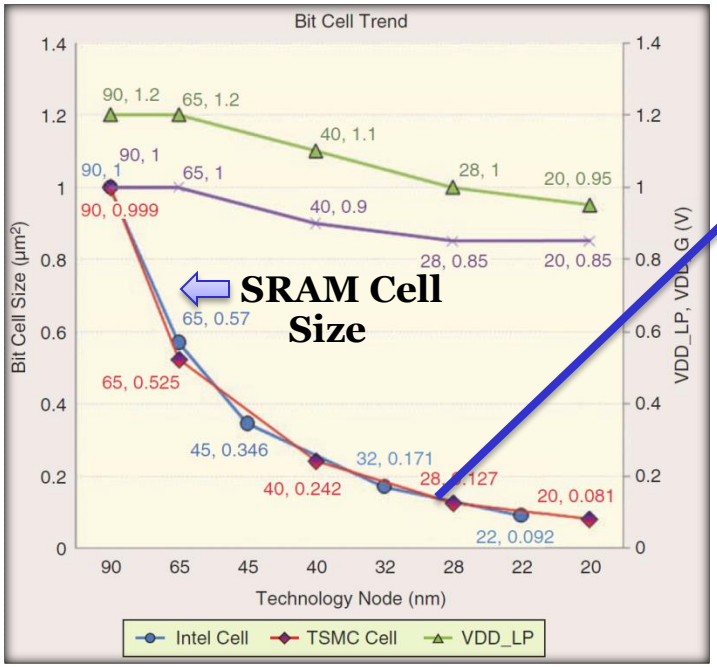
Outline

- Motivation
- Bi-Layer xGNR Device, Latch
- Proposed Memory Cell - Ternary GNTRAM
- Evaluation and Comparison with CMOS SRAM
- Summary

Multistate Memory: Motivation & Vision

SRAM Area Trends



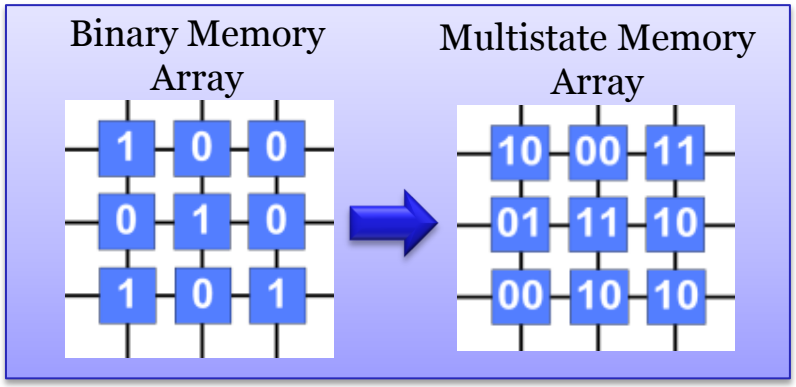
Source: 2012 ISSCC Tech Trends

Vision – New multi-bit per cell volatile memory with graphene

Challenges with CMOS SRAM

- Slowdown in area scaling (50% down to 30% per generation)
- Increasing leakage concerns

Concept



Current: Single bit/cell

Proposed: Multi-bit/cell with novel graphene structures

Bi-Layer Graphene Nanoribbon Crossbar Device (xGNR) & Application

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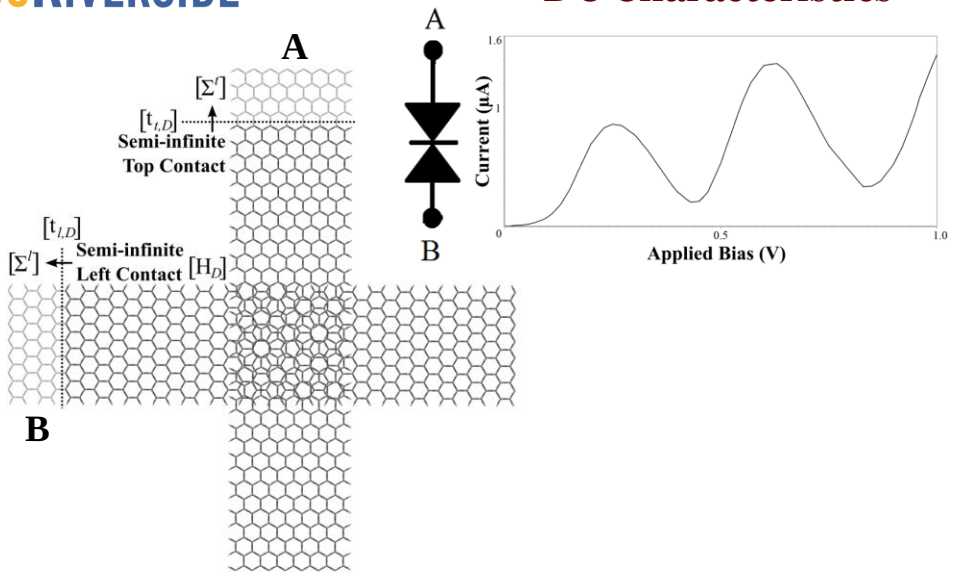
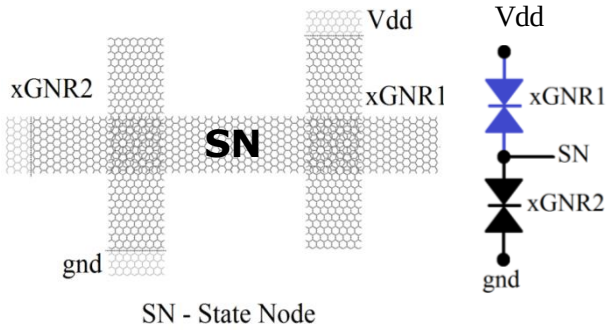
DC Characteristics



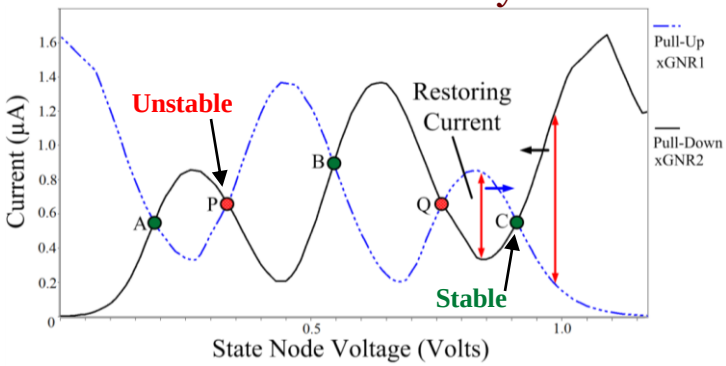
Graphene Nanoribbon Crossbar Resonant Tunneling Diode - *K. M. M. Habib and R. K. Lake*, University of California Riverside

Latch Configuration

UMASS AMHERST



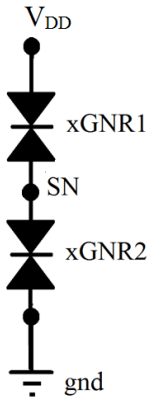
DC Load Line Analysis



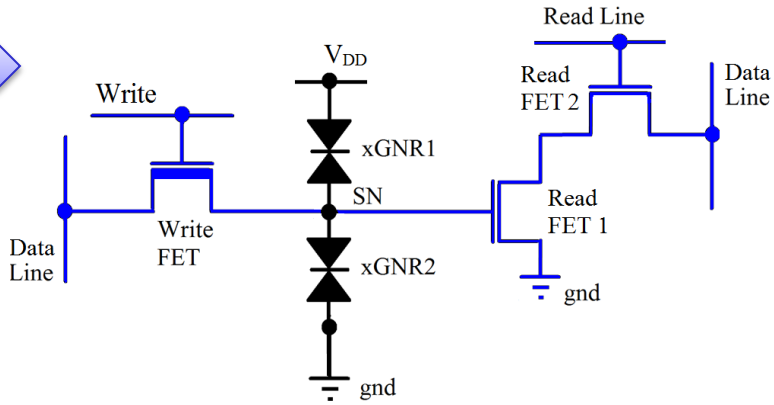
- Armchair Graphene Nano-Ribbons arranged in a crossbar geometry (xGNR) exhibit Negative Differential Resistance (NDR)
- xGNRs in series form a latch with multiple stable states (A, B & C)
- Ternary data represented by state node (SN) voltage: A—Logic 0, B—Logic 1, & C—Logic 2

Graphene Nanoribbon Tunneling RAM (GNTRAM)

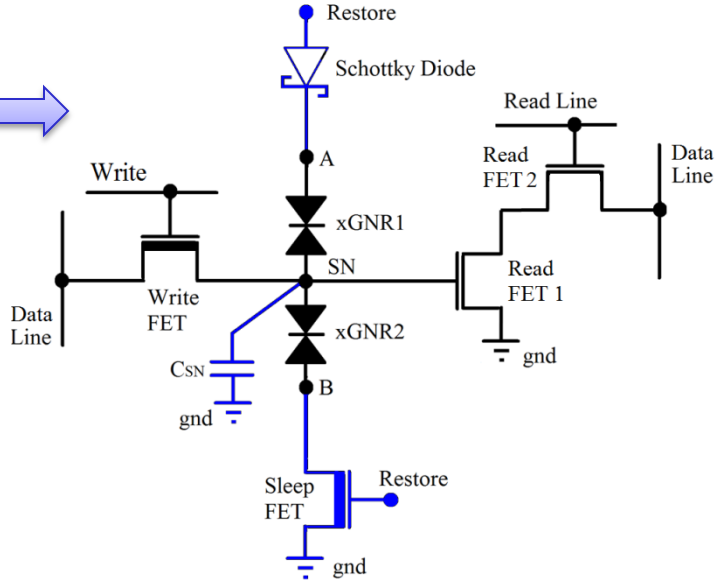
xGNR Latch



Memory Circuit



Proposed Memory Cell

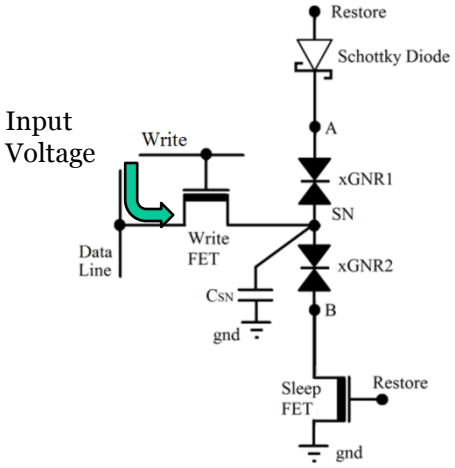


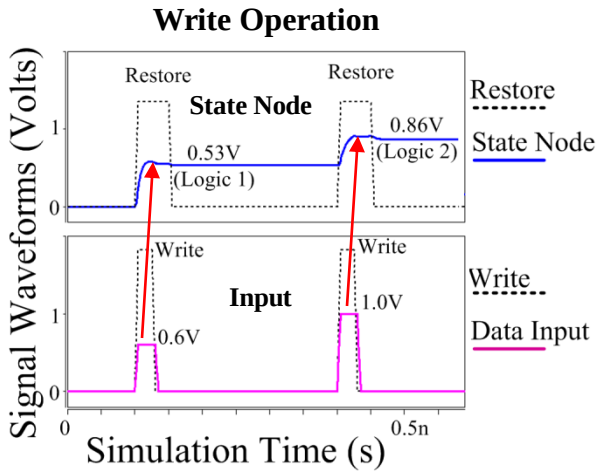
SN - State Node

- xGNR latch forms the memory core of a RAM cell
- Memory cell selection, read and write operations performed using access transistors
- Schottky diode and Sleep FET mitigate stand-by power consumption

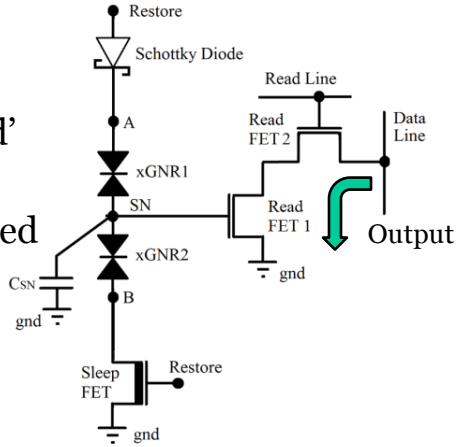
Ternary GNTRAM Operation

- Write Operation:
  - Ternary data represented by state node (SN) voltage
  - Apply input voltage on 'Data Line' & assert 'Write' signal
  - Charge/discharge state node to required voltage

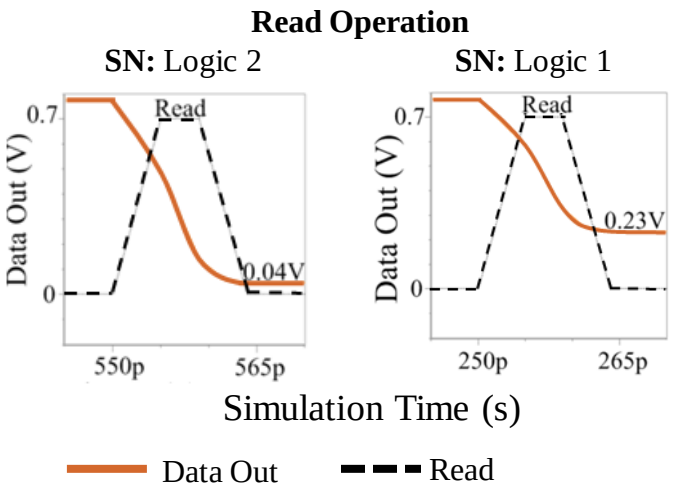




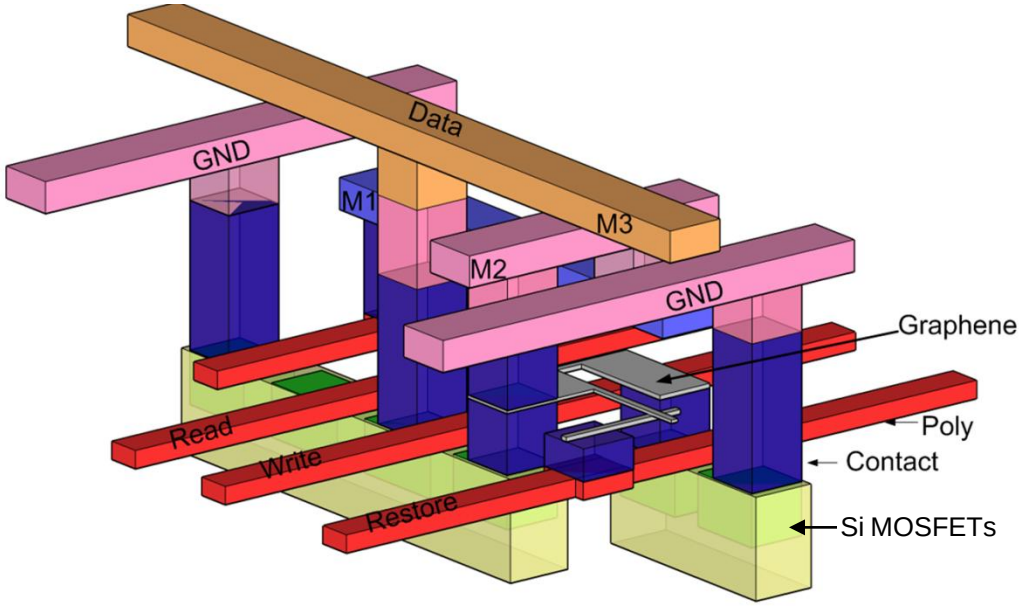
- Read Operation:
  - Pre-charge 'Data Line' & apply 'Read' pulse
  - Output is pulled down based on stored logic state
  - Non-destructive read

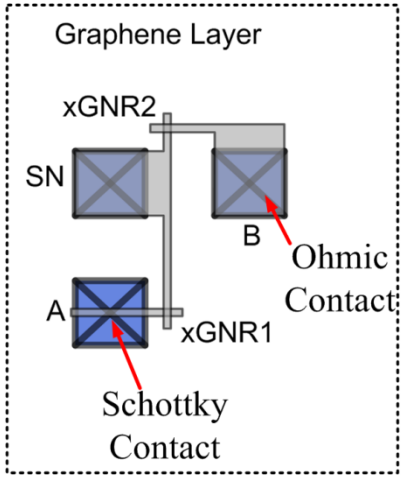


SN - State Node



Proposed Physical Implementation – Integration with CMOS





- Heterogeneous integration between CMOS and Graphene for validation and benchmarking
- MOS transistors and metal layers for access and routing
- Schottky contact* enabled by interaction between semiconducting GNR and metal

*X. Guan; et al.; , "**Modeling of schottky and ohmic contacts between metal and graphene nanoribbons using extended hückel theory (EHT)-based NEGF method**," IEDM 2008.

Methodology & Benchmarking

- HSPICE simulation for concept validation, performance and power evaluation
- 16nm Grid-based design rules used to evaluate GNTRAM area

16nm Design Rules

1D Gridded Design	*M1, M2 Interconnect*	*Poly*
Pitch (16nm technology node)	40~60 nm	60~80nm

C. Bencher, et al.. "**Gridded design rule scaling: Taking the CPU toward the 16nm node**", Proc. SPIE 7274, 2009

Comparison with 16nm High Performance (HP) CMOS SRAM

	GNT RAM (Per Cell, 1.585 bits)	***GNT RAM (Per Bit)***	*CMOS 6T Scaled SRAM Cell*	*CMOS Gridded 8T SRAM Cell*
RAM Cell Area (μm²)	0.03-0.06	**0.019-0.038**	0.026-0.064	0.034-0.067
Active Power (μW)	2.1	**1.31**	2.1	2.41
Standby Power (pW)	22	**13.9**	6152	15552

Performance	***GNT RAM***	*CMOS 6T Scaled SRAM Cell*	*CMOS Gridded 8T SRAM Cell*
Read Time (ps)	**9.3**	8.8	7.7
Write Time (ps)	**16.3**	18.4	18

Density Benefit (per bit) : Upto 1.77x vs. SRAMs
Power Savings (per bit): Upto 1.84x (Active) and 1196x (Leakage) vs. HP SRAMs
Performance: Comparable to HP CMOS SRAMs

Summary

- Novel ternary memory (1.5 bits/cell) presented with heterogeneous CMOS-Graphene implementation
- Density and power benefits vs. 16nm CMOS SRAMs with comparable performance
- Next Steps: Increasing number of states/cell – *a new dimension for scaling*
- Possibility of all-graphene fabrics as graphene technology matures

Thank You!

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